Amendment to the Drawings

The attached sheets of drawings include changes to Figs. 1, 2, and 3. These sheets, which include Figs. 1, 2, and 3, replace the original sheets including Figs. 1, 2, and 3.

Fig. 1 – The legend "Prior Art" has been added.

Fig. 2 – The lead line for element 203 has been correct.

Fig. 3 – The reference numeral for delay circuit 316 in frequency offset calculator 306 has been corrected.

Attachments: Replacement sheets

Annotated sheets showing changes

REMARKS

Applicants have reviewed the Office Action mailed on October 16, 2006 as well as the art cited. Claims 1-3, and 5-21 are pending in this application. Claims 1, 8, 10, 15, and 17 have been amended. Claim 4 has been cancelled.

Objections to the Drawings

Figures 1 and 2 have been amended to correct the typographical errors noted by the Examiner. In addition, Figure 3 has been amended to correct a typographical error in a reference numeral. In amending Figures 1-3, no new matter has been added.

Objections to the Specification

Paragraph [0011] of the Background section has been amended to identify the quantities Zq(t) and Zi(t) as required by the Examiner. In addition, paragraph [0034] has been amended to correct a typographical error in a reference numeral. In amending paragraphs [0011] and [0034] no new mater has been added.

Rejections Under 35 U.S.C. § 103

Claims 1-3, 5, 7-9, 11-12, 14-16, 18-19, and 21 were rejected under 35 USC § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Dutta (U.S. Patent No. 5,313,493) (hereinafter referred to as Dutta) in further view of Chung et al. (U.S. Publication No. 2004/0190655) (hereinafter referred to as Chung). Applicants respectfully traverse these rejections.

Claim 1 recites:

1. A differential phase shift keying (DPSK) receiver to receive a DPSK signal transmitted by a DPSK transmitter, comprising:

means for converting the input signal to in-phase and quadrature components;

a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components with a first delayed, conjugated version of the in-phase and quadrature components;

a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components;

a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase;

a phase correction circuit to determine an absolute phase using the corrected phase; and

a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data.

Applicants assert that nothing in the AAPA, Chung et al or Dutta, taken alone or together, teaches or suggests "a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components."

In addressing the above limitation in claim 1, the Examiner asserted that Chung et al teaches "a frequency offset calculation circuit to determine a frequency offset by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 5. In support of this assertion, the Examiner refers to paragraph 0005 of Chung. However, paragraph 5 merely discusses "a phase-increment extraction circuit 40" which "includes a delay circuit 41, a conjugate circuit 42, and a multiplier 45." The phase-increment extraction circuit 40 outputs "the phasor R_k" which "has an argument containing ***the phase increment*** $\Delta\theta$ rotated according to frequency offsets and the phase

difference of successive samples of the modulation." (emphasis added). Para. [0005]. In addition, Chung discusses in paragraph 0005 "the argument circuit 30 extracts the phase offset" and "the frequency offset f ***can be estimated*** by using the phase offset of the phasor R_k".

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para. [0007] (emphasis added). Hence, the phase-increment extraction circuit in Chung does not teach or suggest a "frequency offset calculation circuit frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components ***with a second*** delayed, conjugated version of the in-phase and quadrature components." At best, the phase-increment extraction circuit of Chung et al. teaches a differential demodulator as discussed in the background section of the present application. Since nothing in Chung et al., the AAPA, or Dutta, taken alone or in combination, teaches or suggests all the claimed limitations of claim 1, claim 1 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 2-3, and 5-7 depend from claim 1 and, thus, are allowable for at least the reasons stated above with respect to claim 1. Applicants, therefore, request that the rejections be withdrawn.

Claim 8 recites:

8. A method for demodulating a differential phase shift keying (DPSK) signal, comprising:

receiving the DPSK signal;

digitizing the DPSK signal;

converting the DPSK signal into its corresponding in-phase (I) and quadrature (Q) components;

filtering the I and Q components to remove noise;

determining a phase associated with the I and Q components by comparing the I and Q components to a first delayed and conjugated version of the I and Q components;

determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components;

adjusting the determined phase using the determined frequency offset;

converting the adjusted phase to an absolute phase; and

mapping the absolute phase to a symbol corresponding to one or more data bits.

Applicants assert that nothing in the AAPA, Chung et al or Dutta, taken alone or together, teaches or suggests "determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components."

In addressing the above limitation in claim 8, the Examiner referred to arguments made above with respect to claim 1. In particular, the Examiner asserted that Chung et al teaches "a frequency offset calculation circuit to determine a frequency offset by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 5. In support of this assertion, the Examiner refers to paragraph 0005 of Chung. However, paragraph 5 merely discusses "a phase-increment extraction circuit 40" which "includes a delay circuit 41, a conjugate circuit 42, and a multiplier 45." The phase-increment extraction circuit 40 outputs "the phasor R_k" which "has an argument containing ***the phase increment*** $\Delta\theta$ rotated according to frequency offsets and the phase difference of successive samples of the modulation." (emphasis added). Para. [0005]. In addition, Chung discusses in paragraph 0005 "the argument circuit 30 extracts the phase offset" and "the frequency offset f ***can be estimated*** by using the phase offset of the phasor R_k".

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para.

[0007] (emphasis added). Hence, at best, the phase-increment extraction circuit of Chung et al. teaches a differential demodulator as discussed in the background section of the present application. Nothing in Chung et al. teaches or suggests "determining a frequency offset associated with the I and Q components by comparing the I and Q components to ***a second*** delayed and conjugated version of the I and Q components." Since nothing in Chung et al., the AAPA, or Dutta, taken alone or in combination, teaches or suggests all the claimed limitations of claim 8, claim 8 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 9-14 depend from claim 8 and, thus, are allowable for at least the reasons stated above with respect to claim 8. Applicants, therefore, request that the rejections be withdrawn.

Claim 15 recites:

15. A system for demodulating a differential phase shift keying (DPSK) signal, comprising:

means for converting the DPSK signal into its corresponding in-phase (I) and quadrature (Q) components;

means for filtering the I and Q components to remove noise;

means for determining a phase associated with the I and Q components by comparing the I and Q components to a first delayed and conjugated version of the I and Q components;

means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components;

means for adjusting the determine phase using the determined frequency offset;

means for converting the adjusted phase to an absolute phase; and

means for mapping the absolute phase to a symbol corresponding to one or more data bits.

Applicants assert that nothing in the AAPA, Chung et al or Dutta, taken alone or together, teaches or suggests "means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components."

In addressing the above limitation in claim 15, the Examiner referred to arguments made above with respect to claim 1. In particular, he Examiner asserted that Chung et al teaches "a frequency offset calculation circuit to determine a frequency offset by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 5. In support of this assertion, the Examiner refers to paragraph 0005 of Chung. However, paragraph 5 merely discusses "a phase-increment extraction circuit 40" which "includes a delay circuit 41, a conjugate circuit 42, and a multiplier 45." The phase-increment extraction circuit 40 outputs "the phasor R_k" which "has an argument containing ***the phase increment*** $\Delta\theta$ rotated according to frequency offsets and the phase difference of successive samples of the modulation." (emphasis added). Para. [0005]. In addition, Chung discusses in paragraph 0005 "the argument circuit 30 extracts the phase offset" and "the frequency offset f ***can be estimated*** by using the phase offset of the phasor R_k".

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para. [0007] (emphasis added). Hence, the phase-increment extraction circuit in Chung does not teach or suggest a "means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to ***a second*** delayed and conjugated version of the I and Q components." At best, the phase-increment extraction circuit of Chung et al. teaches a differential demodulator as discussed in the background section of the present application. Since nothing in Chung et al., the AAPA, or Dutta, taken alone or in combination, teaches or suggests all the claimed limitations of claim 15, claim 15 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 16-21 depend from claim 15 and, thus, are allowable for at least the reasons stated above with respect to claim 15. Applicants, therefore, request that the rejections be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 1, 3-5, 8-10, 12, 15, and 17 were rejected under 35 USC § 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of LaBerge et al. (U.S. Patent No. 5,142,287) (hereinafter referred to as LaBerge). Applicants respectfully traverse these rejections.

Claim 1 recites:

1. A differential phase shift keying (DPSK) receiver to receive a DPSK signal transmitted by a DPSK transmitter, comprising:

means for converting the input signal to in-phase and quadrature components;

a differential demodulator to determine a demodulated phase by comparing the in-phase and quadrature components with a first delayed, conjugated version of the in-phase and quadrature components;

a frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components;

a frequency correction circuit to correct the demodulated phase using the frequency offset into a corrected phase;

a phase correction circuit to determine an absolute phase using the corrected phase; and

a symbol mapping circuit to map the absolute phase to an output symbol, comprising one or more bits of data.

Applicants assert that nothing in the AAPA, or LaBerge et al., taken alone or together, teaches or suggests "a frequency offset calculation circuit to determine a frequency offset

between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components."

In addressing the above limitation in claim 1, the Examiner asserted that LaBerge et al discloses "a frequency offset calculation circuit to determine a frequency offset between the DPSK receiver and the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 9. In support of this assertion, the Examiner refers to the abstract, col. 5 lines 43-44, col. 4 lines 56-64, and col. 6 lines 42-45. In addition, the Examiner refers to "the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector)" in Fig. 7. However, LaBerge el al. merely discusses "one of the advantages of the present invention is the removal of the effects of the unknown rotation wT. This is achieved by the application of the complex phase correction/rotation factor, r(t), ***after the DPSK demodulation process***." col. 5 lines 43-47. With regards to phase correction/rotation factor r(t), LaBerge states "the complex output of ***low pass filter 21*** establishes a 'reference' estimate, r(t)." In addition, with regards to elements 15, 16, and 17 of Fig. 7, LaBerge states "this series of operations results in a sequence of complex values whose phase angles are a measure of the ***phase difference*** between two consecutive DPSK bits."

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para. [0007] (emphasis added). Hence, the cited passages and elements 15, 16, and 17 in LaBerge et al. do not teach or suggest a "frequency offset calculation circuit frequency offset calculation circuit to determine a frequency offset between an oscillator in the DPSK receiver and an oscillator in the DPSK transmitter by comparing the in-phase and quadrature components ***with a second*** delayed, conjugated version of the in-phase and quadrature components." At best, elements 15, 16, and 17 teach a differential demodulator as discussed in the background section of the present application. Since nothing in Laberge et al. or the AAPA, taken alone or in

combination, teaches or suggests all the claimed limitations of claim 1, claim 1 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 2-3, and 5-7 depend from claim 1 and, thus, are allowable for at least the reasons stated above with respect to claim 1. Applicants, therefore, request that the rejections be withdrawn.

Claim 8 recites:

8. A method for demodulating a differential phase shift keying (DPSK) signal, comprising:

receiving the DPSK signal;

digitizing the DPSK signal;

converting the DPSK signal into its corresponding in-phase (I) and quadrature (Q) components;

filtering the I and Q components to remove noise;

determining a phase associated with the I and Q components by comparing the I and Q components to a first delayed and conjugated version of the I and Q components;

determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components;

adjusting the determined phase using the determined frequency offset;

converting the adjusted phase to an absolute phase; and

mapping the absolute phase to a symbol corresponding to one or more data bits.

Applicants assert that nothing in the AAPA, or LaBerge et al., taken alone or together, teaches or suggests "determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components."

In addressing the above limitation in claim 8, the Examiner referred to arguments made above with respect to claim 1. In particular, the Examiner asserted that LaBerge et al discloses "a frequency offset calculation circuit to determine a frequency offset between the DPSK receiver and the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 9. In support of this assertion, the Examiner refers to the abstract, col. 5 lines 43-44, col. 4 lines 56-64, and col. 6 lines 42-45. In addition, the Examiner refers to "the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector)" in Fig. 7. However, LaBerge el al. merely discusses "one of the advantages of the present invention is the removal of the effects of the unknown rotation wT. This is achieved by the application of the complex phase correction/rotation factor, r(t), ***after the DPSK demodulation process***." col. 5 lines 43-47. With regards to phase correction/rotation factor r(t), LaBerge states "the complex output of ***low pass filter 21*** establishes a 'reference' estimate, r(t)." In addition, with regards to elements 15, 16, and 17 of Fig. 7, LaBerge states "this series of operations results in a sequence of complex values whose phase angles are a measure of the ***phase difference*** between two consecutive DPSK bits."

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para. [0007] (emphasis added). Hence, the cited passages and elements 15, 16, and 17 in LaBerge et al., at best, teach a differential demodulator as discussed in the background section of the present application. Since nothing in Laberge et al. or the AAPA, taken alone or in combination, teaches or suggests all the claimed limitations of claim 8, claim 8 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 9-14 depend from claim 8 and, thus, are allowable for at least the reasons stated above with respect to claim 8. Applicants, therefore, request that the rejections be withdrawn.

Claim 15 recites:

15. A system for demodulating a differential phase shift keying (DPSK) signal, comprising:

means for converting the DPSK signal into its corresponding in-phase (I) and quadrature (Q) components;

means for filtering the I and Q components to remove noise;

means for determining a phase associated with the I and Q components by comparing the I and Q components to a first delayed and conjugated version of the I and Q components;

means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components;

means for adjusting the determine phase using the determined frequency offset;

means for converting the adjusted phase to an absolute phase; and

means for mapping the absolute phase to a symbol corresponding to one or more data bits.

Applicants assert that nothing in the AAPA, or LaBerge et al., taken alone or together, teaches or suggests "means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components."

In addressing the above limitation in claim 15, the Examiner referred to arguments made above with respect to claim 1. In particular, the Examiner asserted that LaBerge et al discloses "a frequency offset calculation circuit to determine a frequency offset between the DPSK receiver and the DPSK transmitter by comparing the in-phase and quadrature components with a second delayed, conjugated version of the in-phase and quadrature components." OA p. 9. In support of this assertion, the Examiner refers to the abstract, col. 5 lines 43-44, col. 4 lines 56-64, and col. 6 lines 42-45. In addition, the Examiner refers to "the use of elements 15 (one bit delay), 16 (conjugate), 17 (coherent detector)" in Fig. 7. However, LaBerge el al. merely discusses "one of the advantages of the present invention is the removal of the effects of the

unknown rotation wT. This is achieved by the application of the complex phase correction/rotation factor, r(t), ***after the DPSK demodulation process***." col. 5 lines 43-47. With regards to phase correction/rotation factor r(t), LaBerge states "the complex output of ***low pass filter 21*** establishes a 'reference' estimate, r(t)." In addition, with regards to elements 15, 16, and 17 of Fig. 7, LaBerge states "this series of operations results in a sequence of complex values whose phase angles are a measure of the ***phase difference*** between two consecutive DPSK bits."

Similarly, in an "exemplary conventional DPSK demodulator" discussed in the background section of the present application "the current symbol is compared to the prior symbol to determine relative ***phase difference*** between the current and previous symbols." Para. [0007] (emphasis added). Hence, the cited passages and elements 15, 16, and 17 in LaBerge et al. do not teach or suggest "means for determining a frequency offset associated with the I and Q components by comparing the I and Q components to a second delayed and conjugated version of the I and Q components." At best, elements 15, 16, and 17 teach a differential demodulator as discussed in the background section of the present application. Since nothing in Laberge et al. or the AAPA, taken alone or in combination, teaches or suggests all the claimed limitations of claim 15, claim 15 is not obvious. Therefore, Applicants request that the rejection be withdrawn.

Claims 16-21 depend from claim 15 and, thus, are allowable for at least the reasons stated above with respect to claim 15. Applicants, therefore, request that the rejections be withdrawn.

CONCLUSION

Applicant respectfully submits that claims **1-21** are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

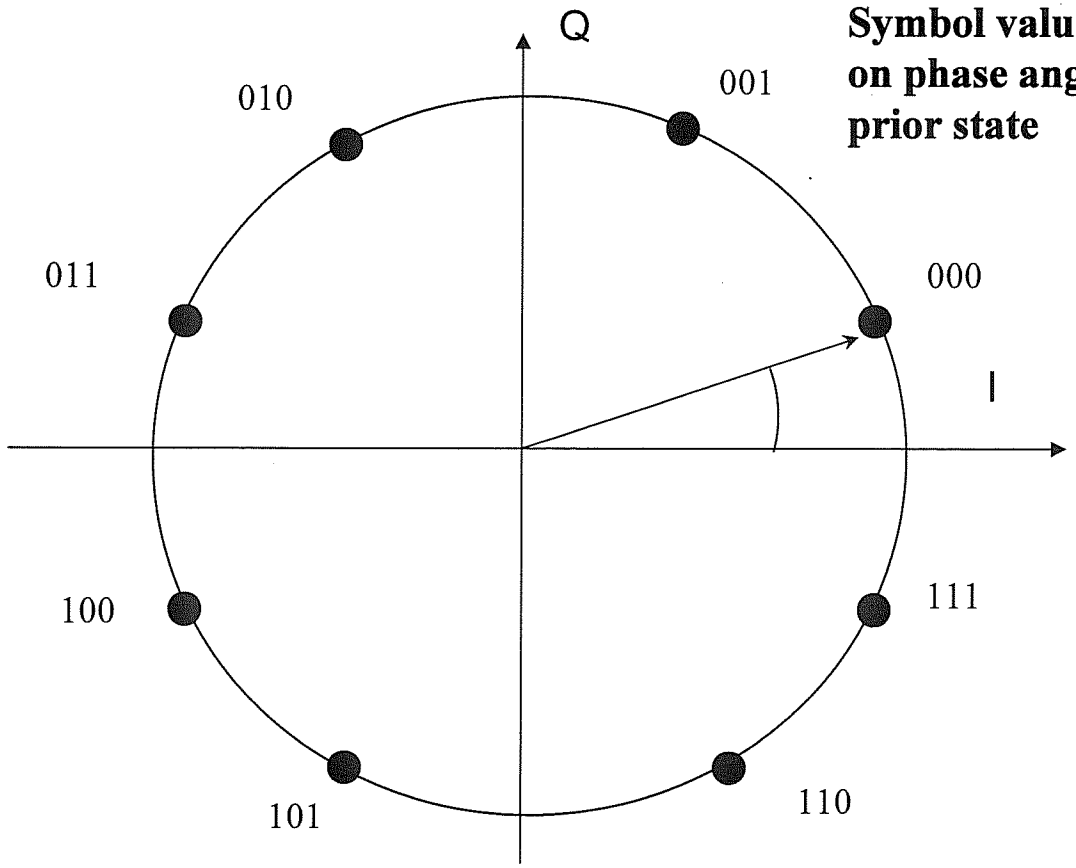
/David N. Fogg/

Date: January 16, 2007

David N. Fogg
Reg. No. 35,138

Attorneys for Applicant
Fogg and Associates, LLC
P.O. Box 581339
Minneapolis, MN 55458-1339
T – (612) 332-4720
F – (612) 332-4731

Attachments



Symbol value of symbol depends on phase angle difference from prior state

Figure 1
(Prior Art)

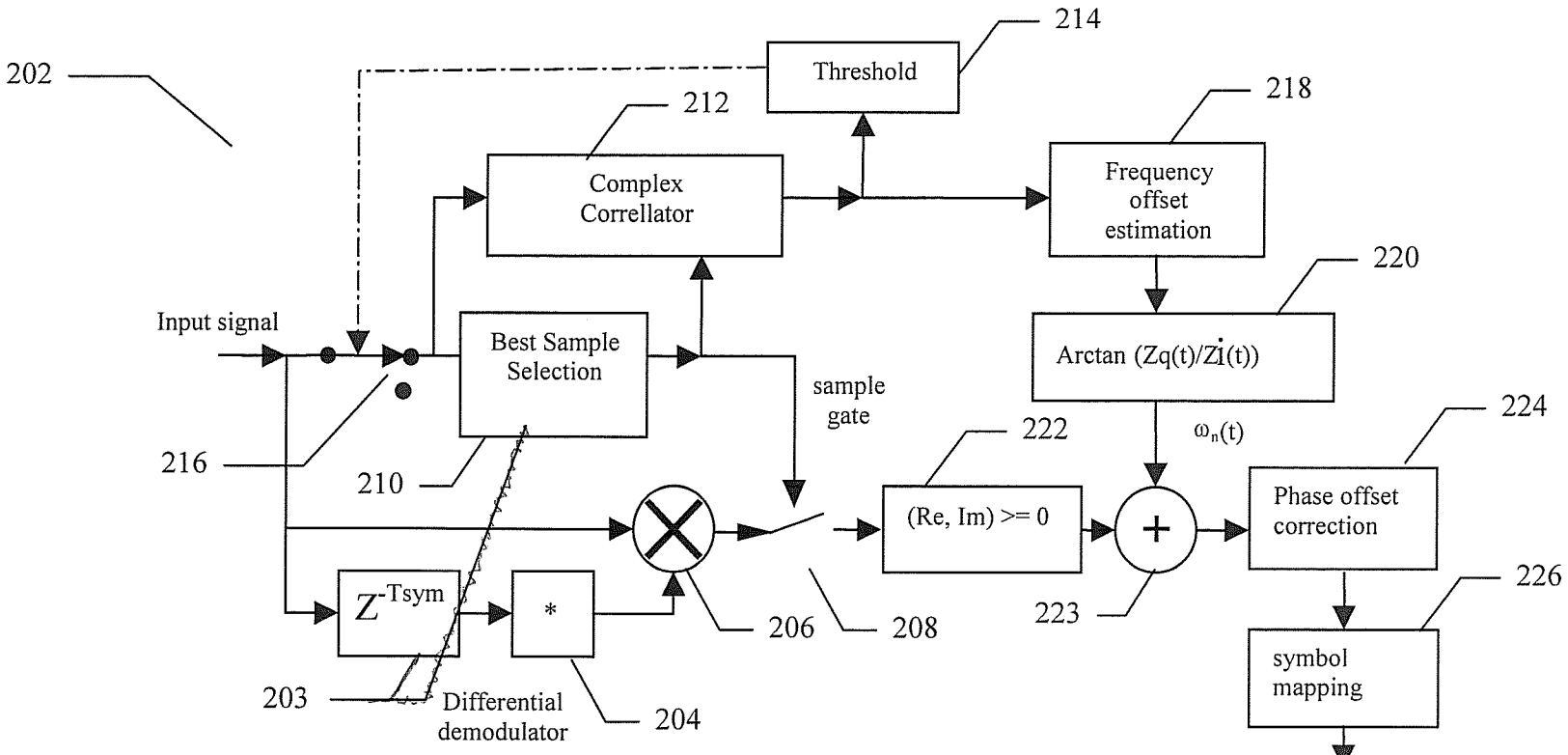


Figure 2
(PRIOR ART)

Title: COMPUTATIONALLY EFFICIENT DEMODULATION FOR DIFFERENTIAL PHASE SHIFT KEYING
Serial No. 10/615,880 Attorney Docket No. H0004522-5601
ANNOTATED SHEET

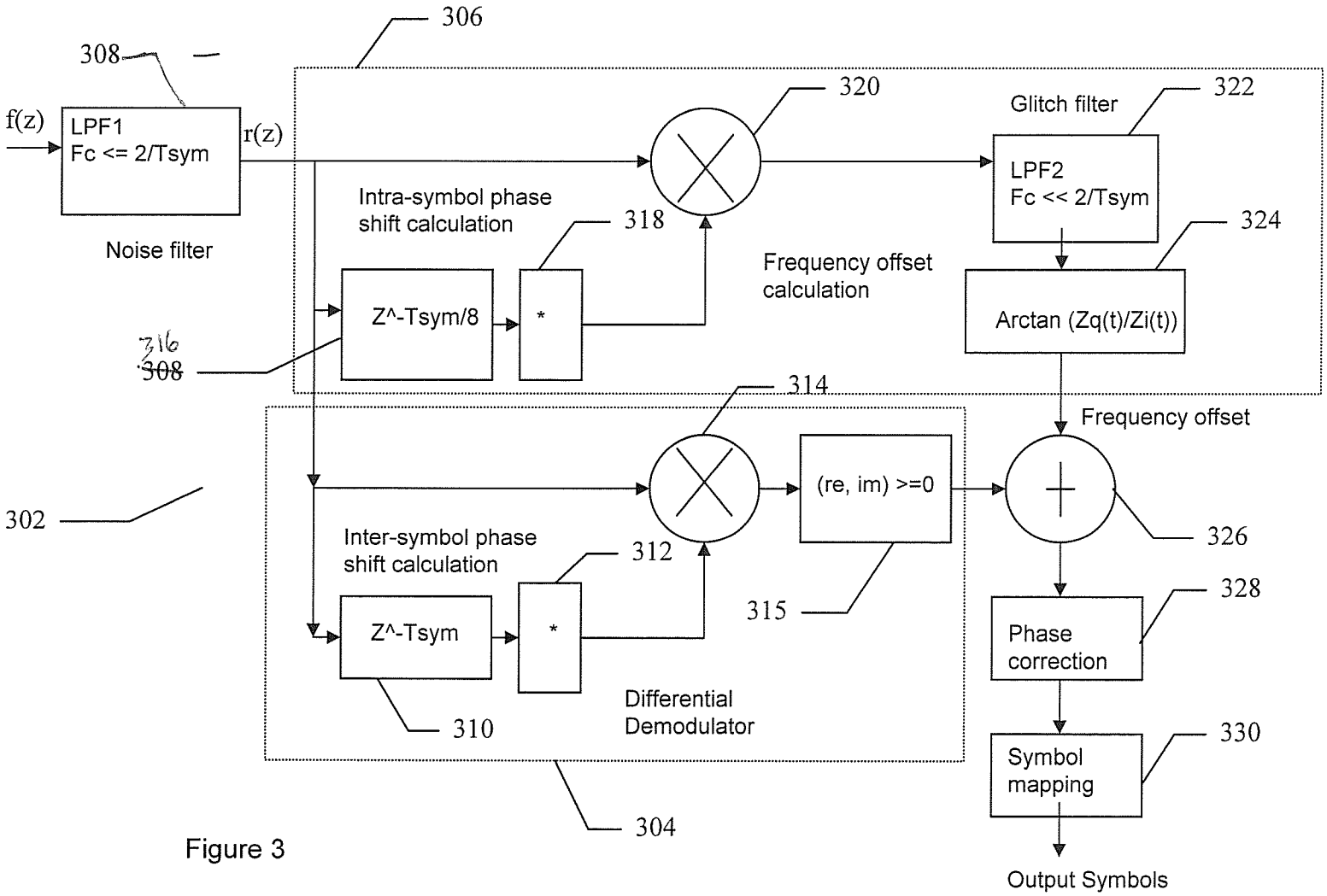


Figure 3

Title: COMPUTATIONALLY EFFICIENT DEMODULATION
FOR DIFFERENTIAL PHASE SHIFT KEYING
Serial No. 10/615,880 Attorney Docket No. H0004522-5601
ANNOTATED SHEET